REMARKS

Claims 1-24 are all the claims presently pending in this application. Claims 1-2, 13-14 and 16 have been amended to more particularly define the claimed invention.

It is noted that the amendments are made only to more particularly define the invention and **not** for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability. It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Houssein, U.S. Pat. No. 6,418,479, further in view of Kauffman, U.S. Pat. No. 6,633,916.

This rejection is respectfully traversed in view of the following discussion.

I. APPLICANT'S CLAIMED INVENTION

The claimed invention (as defined, for example, by independent claim 1) is directed to a clustered computer system including, a plurality of central processing units (CPU) and memory installed apparatuses having at least one CPU and at least one memory; a plurality of input/output control apparatuses; and a plurality of diagnostic control circuits, each diagnostic control circuit of the plurality of diagnostic control circuits is connected with one of the plurality of the CPU and memory installed apparatus, with one of the plurality of input/output control apparatuses, and each of the plurality of diagnostic control circuits are connected to one another, wherein the CPU and memory installed apparatuses and the input/output control apparatuses are connected to each other by a network, wherein the CPU and memory installed

apparatuses transmit an input/output instruction to at least one of the plurality of input/output control apparatuses assigned in advance, and wherein when the plurality of diagnostic control circuits detect a fault in a connected CPU and memory installed apparatus, the plurality of diagnostic control circuits retrieve previously stored information that determines a new connection between a non-faulty CPU and memory installed apparatus with the input/output control apparatus originally connected to a faulty CPU and memory installed apparatus.

Conventionally, the problem of a conventional computer system is that when a CPU or memory of computer system fails and cannot be used, even if input/output control circuit in the faulty computer system is free of any fault and hence is normal, the normal input/output control circuit and peripheral devices under its control cannot be used. The reason for this problem is that in a conventional computer system the input/output control circuit can only be controlled from a CPU that is connected thereto through the control circuit, and the CPU and the input/output control circuit which carries out input/output instructions issued by the CPU are assembled on same board, which is a minimum unit for maintenance and replacement. (Application at page 3, line 23 to page 4, line 10.)

In the claimed invention (e.g., as recited in claims 1, 13-14 and 16), on the other hand, "*a plurality of diagnostic control circuits, each diagnostic control circuit of said plurality of diagnostic control circuits being connected with one of said plurality of the CPU and memory installed apparatus, with one of said plurality of input/output control apparatuses, and each of said plurality of diagnostic control circuits being connected to one another*," and "*wherein when said plurality of diagnostic control circuits detect a fault in a connected CPU and memory installed apparatus, said plurality of diagnostic control circuits retrieve previously stored information that determines a new connection between a non-faulty CPU and memory*

installed apparatus with said input/output control apparatus originally connected to a faulty CPU and memory installed apparatus." This feature is important to increase the availability of a computer system upon a fault thereof. (Application at page 4, lines 11-13, and page 34, line 25 to page 35, line 22.)

II. THE PRIOR ART REJECTION

The 35 U.S.C. § 103(a) Rejection over Houssein, U.S. Pat. No. 6,418,479 further in view of Kauffman, U.S. Pat. No. 6,633,916

The Examiner alleges that Houssein, U.S. Pat. No. 6,418,479, (Houssein), further in view of Kauffman, U.S. Pat. No. 6,633,916, (Kauffman), makes obvious the invention of claims 1-24.

The Examiner alleges that one of ordinary skill in the art would have been motivated to modify Houssein with the teaching from Kauffman to form the invention of claims 1-24. Applicant submits, however that these references would not have been combined and even if combined, the combination would not teach or suggest each element of the claimed invention.

Indeed, Applicant submits, however, that neither Houssein, nor Kauffman, nor any alleged combination thereof, teaches or suggests, "*a plurality of diagnostic control circuits, each diagnostic control circuit of said plurality of diagnostic control circuits being connected with one of said plurality of the CPU and memory installed apparatus, with one of said plurality of input/output control apparatuses, and each of said plurality of diagnostic control circuits being connected to one another,*" and "*wherein when said plurality of diagnostic control circuits detect a fault in a connected CPU and memory installed apparatus, said plurality of diagnostic control circuits retrieve previously stored information that determines a new connection between a non-faulty CPU and memory installed apparatus with said*

column 4, lines 20-30, wherein the Examiner allegedly attempts to provide motivation to combine Kauffman with Houssein is merely describing the general benefits of the Kauffman reference over that of the prior art – not motivation to combine the teaching of a distributed I/O pass-through system for a computer system (Houssein) with a system for logically and adaptively subdividing partitioning CPUs, memory and I/O ports.

Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner.

Houssein discloses an arrangement for issuing 10 instructions via network, but does not disclose that, when a node becomes faulty, the 10 apparatus that was used by the node, is allocated to another node.

The Examiner admits that Houssein fails to teach or suggest, "*wherein causing said CPU and memory installed apparatuses to transmit an input/output instruction to at least one of said plurality of input/output control apparatuses assigned in advance.*"

Kauffman discloses a method to allocate resources, such as CPU. However, Kauffman fails to disclose or suggest an arrangement wherein nodes are each connected to an 10 apparatus via network, and an allocation of an 10 apparatus is performed among the nodes. In contrast, in the present invention, *a diagnostic control circuit* renders an allocation of an apparatus possible. In order to perform an allocation of an apparatus via network, an arrangement is required wherein information regarding the allocation are centrally managed and the allocation is appropriately performed. The present claimed invention realizes this arrangement through the provision of *a diagnostic control circuit*. Houssein and Kauffman both fail to disclose or suggest this arrangement.

Therefore, Kauffman fails to overcome the deficiencies of Houssein.

Therefore, Applicant respectfully requests the Examiner to reconsider and withdraw this rejection since the alleged prior art references to Houssein and Kauffman (either alone or in combination) fail to teach or suggest each element and feature of Applicant's claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-24, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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